

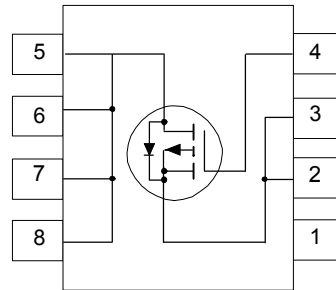
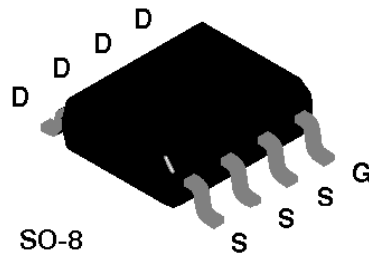
NDS9400A Single P-Channel Enhancement Mode Field Effect Transistor

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.4A, -30V. $R_{DS(ON)} = 0.13\Omega @ V_{GS} = -10V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Rugged and reliable.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS9400A	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	± 3.4	A
	- Pulsed	± 10	
P_D	Maximum Power Dissipation (Note 1a)	2.5	W
		1.2 (Note 1b)	
		1 (Note 1c)	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units		
OFF CHARACTERISTICS								
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V		
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-2	μA		
			$T_J = 55^\circ\text{C}$			-25	μA	
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA		
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA		
ON CHARACTERISTICS (Note 2)								
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$		-1	-1.6	-2.8	V	
			$T_J = 125^\circ\text{C}$	-0.85	-1.25	-2.5		
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}$			0.11	0.13	Ω	
			$T_J = 125^\circ\text{C}$			0.15		0.21
			$V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$			0.17		0.2
			$T_J = 125^\circ\text{C}$		0.24	0.32		
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-10			A		
g_{FS}	Forward Transconductance	$V_{DS} = -15\text{ V}, I_D = -3.4\text{ A}$		4		S		
DYNAMIC CHARACTERISTICS								
C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		350		pF		
C_{oss}	Output Capacitance			260		pF		
C_{rss}	Reverse Transfer Capacitance			100		pF		
SWITCHING CHARACTERISTICS (Note 2)								
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GEN} = -10\text{ V}, R_{GEN} = 6\ \Omega$		9	40	ns		
t_r	Turn - On Rise Time			21	40	ns		
$t_{D(off)}$	Turn - Off Delay Time			21	90	ns		
t_f	Turn - Off Fall Time			8	50	ns		
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V},$ $I_D = -3.4\text{ A}, V_{GS} = -10\text{ V}$		10	25	nC		
Q_{gs}	Gate-Source Charge			1.6		nC		
Q_{gd}	Gate-Drain Charge			3.4		nC		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				-1.9	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -1.25 A (Note 2)		-0.8	-1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _F = -2.0 A, dI _F /dt = 100 A/μs			100	ns
I _{rr}	Reverse Recovery Current			1.9		A

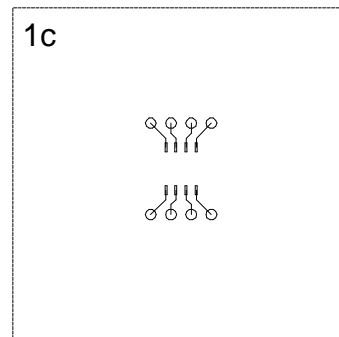
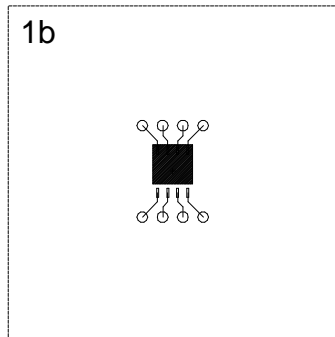
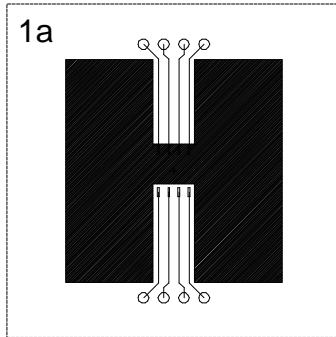
Notes:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J-C}(t)} = \frac{T_J - T_A}{R_{\theta J-C}(t) + R_{\theta C-A}(t)} = I_D^2(t) \times R_{DS(on)} @ T_J$$

Typical R_{θJA} using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 50°C/W when mounted on a 1 in² pad of 2oz copper.
- 105°C/W when mounted on a 0.04 in² pad of 2oz copper.
- 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

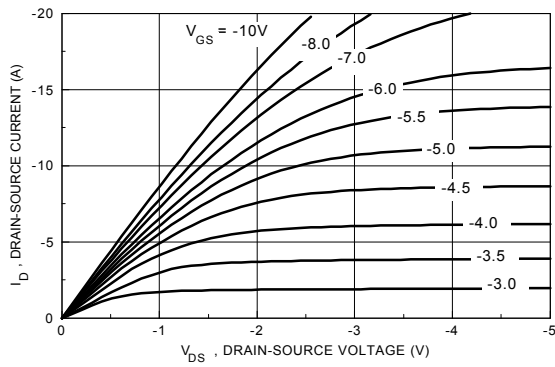


Figure 1. On-Region Characteristics.

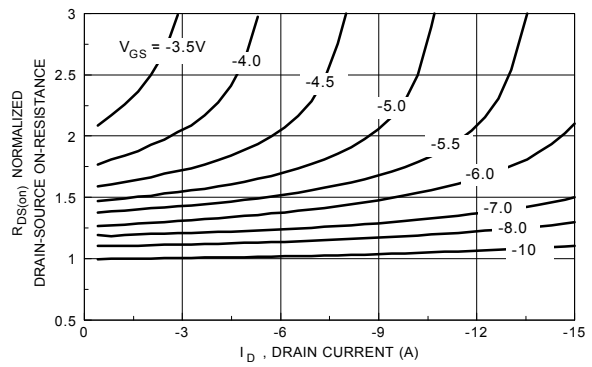


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

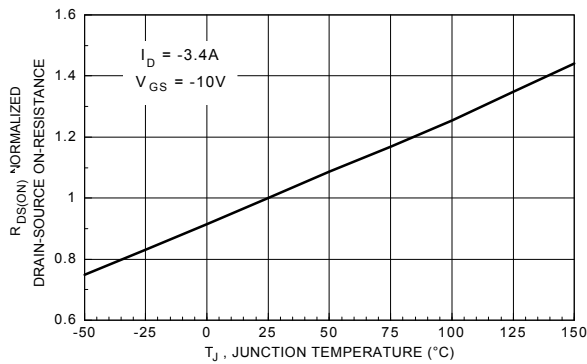


Figure 3. On-Resistance Variation with Temperature.

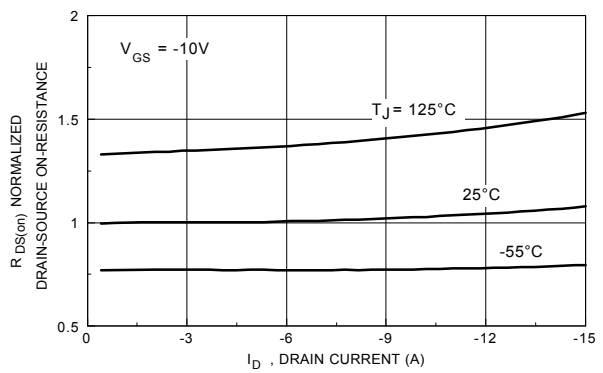


Figure 4. On-Resistance Variation with Drain Current and Temperature.

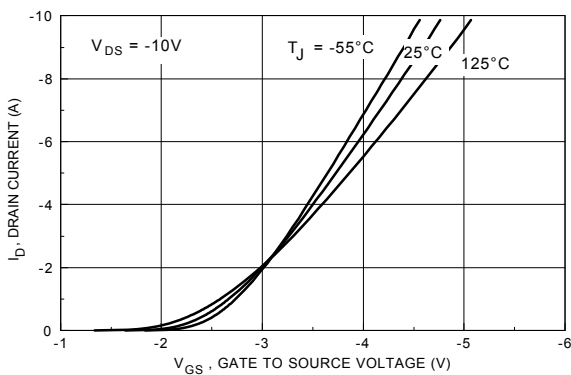


Figure 5. Transfer Characteristics.

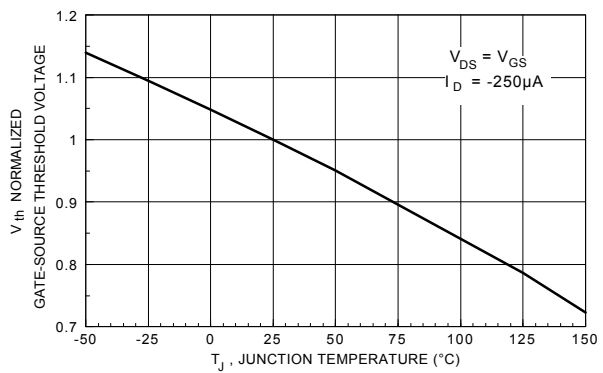


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

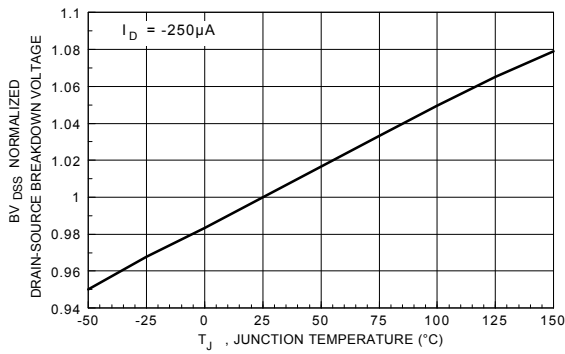


Figure 7. Breakdown Voltage Variation with Temperature.

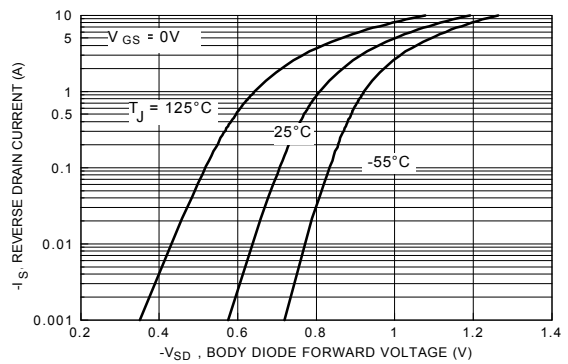


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

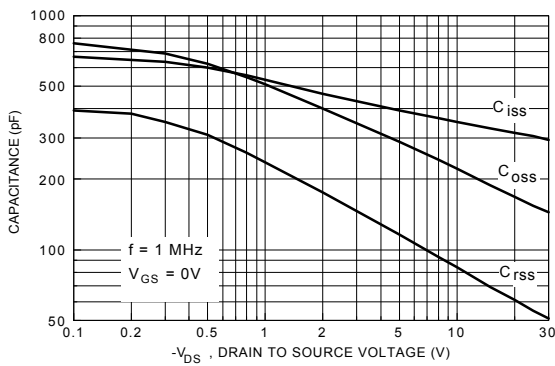


Figure 9. Capacitance Characteristics.

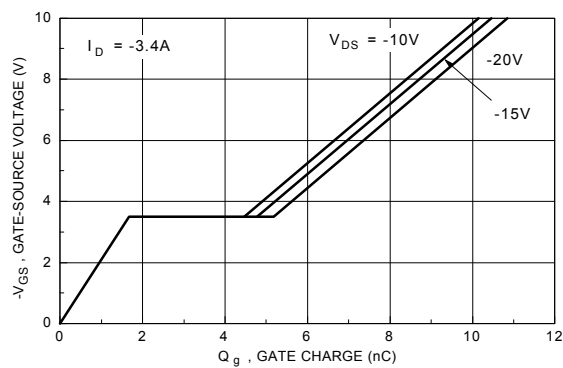


Figure 10. Gate Charge Characteristics.

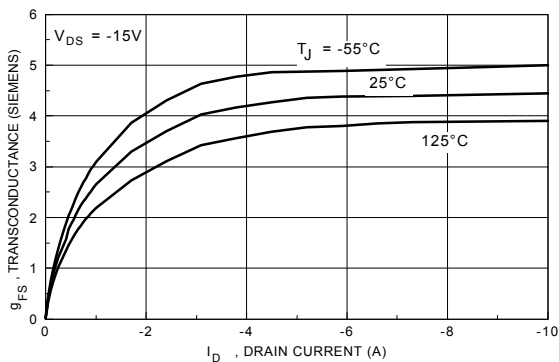


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

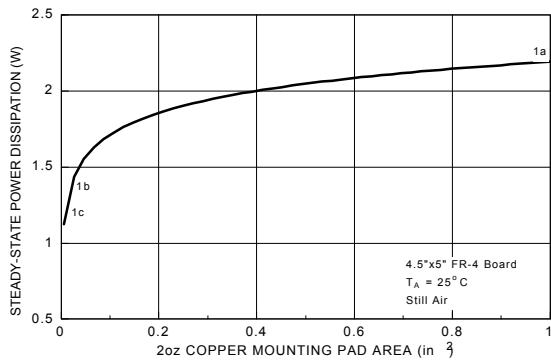


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

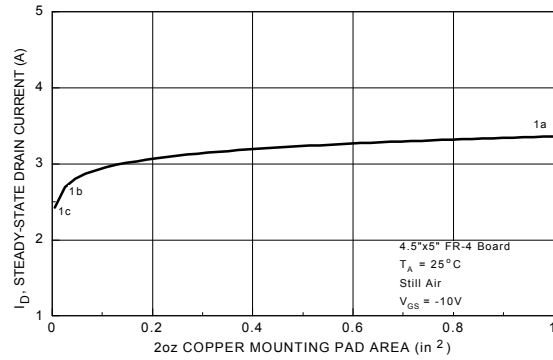


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

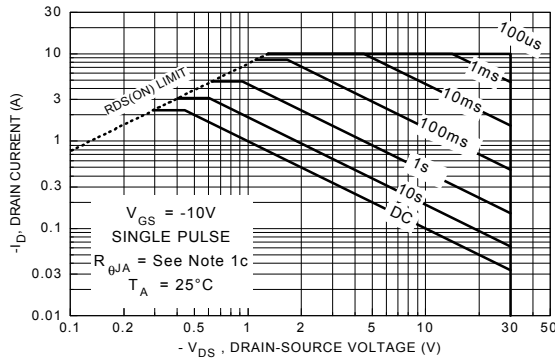


Figure 14. Maximum Safe Operating Area.

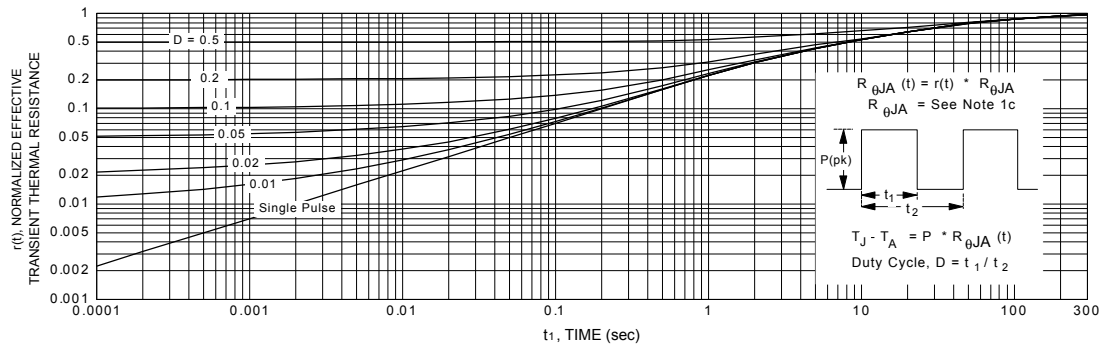


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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